

REMARKS/ARGUMENTS

Applicants note the 3-month shortened statutory period for filing a response to the Office Action expires July 19, 2005 and herein respectfully submit a response thereto. Appropriate fees for a one-month extension of time will be submitted together with this response.

Comments to Amendments to Drawings

The drawings are hereby amended to comply with 37 CFR 1.83(a) and 37 CFR 1.121(d). Basis for amendments to the drawings can be found in the original and amended claims 2 and 21, which are supported by the last paragraph of page 8 of the specification without adding matter.

Rejections of Claims 2 to 20 under 35 USC § 112

In the Office Action, Examiner quoted the second paragraph of 35 USC § 112 which provides that the specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Examiner explains that claim 1 is presently allowed and that claims 2 to 20 are rejected on the basis that these claims were indefinite for failing to point out and distinctly claim the subject matter which applicant regards as the invention. Examiner further explains that claims 2 to 20 would be allowed if rewritten or amended to overcome the rejection under the second paragraph of 35 USC § 112.

Response to Rejections of Claims 2 to 20 under 35 USC § 112

Claims 2 to 12 have been amended to overcome the rejections under 35 USC § 112. The phrase “the current selective D flip-flop circuit” replaces the recitation of “the current selector circuit” in line 1 of each of claims 2 to 11 for providing proper antecedent basis with respect to claim 1. Amended claim 7 is presently dependent on amended claim 5 for providing proper antecedent basis with respect to amended claim 3 and is also amended for a typographical error of the recitation of “the current multiplier”. Amended claim 9 is similarly amended to depend on amended claim 3 for providing proper antecedent basis with respect to amended claim 3.

Claim 12 is amended to include the word “respectively” at the end of the recitation of “applying a first and second current to a first receiving means input terminal of a first receiving means and a second current to a second receiving means input terminal of a second receiving means”. This is for clarifying that a first current is applied to a first receiving means input terminal of a first receiving means and that a second current is applied to a second receiving

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Amendments to the Drawings:

The attached sheet of drawing includes changes to Figure 3. This sheet, which includes Figure 3, replaces the original sheet containing Figure 3.

Attachment: Replacement Sheet

means input terminal of a second receiving means according to Fig. 2 and the last paragraph of page 5 of the present application. Applicants respectfully submit that other 35 U.S.C. §112 rejections for dependent claims 13 to 20 are consequently disposed of and, together with amended claims 2 to 12, are therefore in condition for allowance.

Rejections of Claims 21 and 22 under 35 USC § 102

In the Office Action, Examiner quoted an appropriate paragraph of 35 USC § 102 which provides that a person shall be entitled to a patent unless the invention was anticipated.

Examiner explains that claims 21 and 22 are rejected on the basis that these claims were anticipated by Ichimaru in United States Patent No. 5,661,426.

Response to Rejections of Claims 21 and 22 under 35 USC § 102

Applicants respectfully agree with Examiner that Ichimaru teaches a D flip-flop circuit for high-speed logic operations.

Applicants however respectfully traverse Examiner's statement that Ichimaru teaches "a current selective D flip-flop capable of performing biasing current selection". Conversely, Ichimaru teaches a D flip-flop circuit having a current selecting or switching circuit that consist of a pair of transistor switches which is used for converting clock signals into current signals for the D flip-flop circuit. The current selector circuit is coupled to a master and slave circuit of the D flip-flop circuit. The current switching circuit is therefore used as a current-to-signal converter in the D flip-flop circuit, according to Fig. 2 and lines 65 to 67 of column 4 and the abstract of Ichimaru's patent and is not capable of performing biasing current selection.

For this reason, Applicants respectfully request the withdrawal of the Ichimaru patent as citation for rejecting claims 21 and 22 under 35 USC § 102.

Furthermore, Applicants respectfully submit that claim 21 of the present application has been amended to impart clarity to the description therein, in the event that the Examiner is not persuaded to withdraw the citations of the Ichimaru patent. Amended claim 21 recites a current selective D flip-flop circuit having a different topology from that of the Ichimaru patent. Amended claim 21 specifically describes a current selective D flip-flop circuit capable of performing biasing current selection. The current selective D flip-flop circuit comprises a D flip-flop, a current multiplier coupled to the D flip-flop and a biasing current selector circuit coupled to the current multiplier. The biasing current selector circuit has at least two input terminals for

receiving at least two biasing currents for selecting one of the at least two biasing currents for biasing the D flip-flop, according to the last paragraph of page 5 of the present application.

Ichimaru teaches a D flip-flop circuit having a current switching circuit but does not teach or intimate, according to amended claim 21, a current selective D flip-flop circuit having a biasing current selective circuit that comprises at least two input terminals for receiving at least two biasing currents for selecting one of the at least two biasing currents for biasing the D flip-flop. On the contrary, Ichimaru teaches the use of the current switching circuit for receiving clock signals and converting the clock signals into current signals for logic operations. The current switching circuit as taught by Ichimaru is therefore for serving a different function and purpose when compared with the biasing current selective circuit as recited in amended claim 21.

Additionally, Applicants respectfully submit that the distinctions between the current selective D flip-flop circuit recited in amended claim 21 and the teachings of Ichimaru are apparent, obvious and manifold. Ichimaru teaches use of successive current sources, according to line 14 of column 4 of the Ichimaru patent, for providing a common or fixed biasing current for biasing the D flip-flop. However, Ichimaru but does not provide any means for selecting one of the at least two biasing currents for biasing the D flip-flop as recited in amended claim 21.

The above described merits of the invention results from the unique configuration of the invention as described in amended claim 21. The unique configuration is not taught by Ichimaru and therefore is not anticipated by Ichimaru's patent.

In accordance with the submitted amendments to claim 21 and the accompanying response explaining to the Examiner the distinctions therein over Ichimaru, the rejections under 35 U.S.C. §102 of claim 21 are consequently disposed of and claim 21 is in condition for allowance. Applicants respectfully submit that other 35 U.S.C. §102 rejections for dependent claim 22 are consequently disposed of and dependent claim 22 is therefore in condition for allowance.

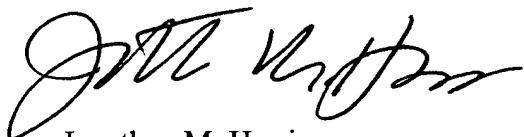
Conclusion

Applicants respectfully request reconsideration and withdrawal of rejections to claims 2 to 20 under 35 U.S.C. § 112 and claims 21 to 22 under 35 U.S.C. § 102 and that a timely Notice of Allowance be issued in this case. Applicants believe a one month extension of time is needed and thus request the time extension. Please charge to Conley Rose, P.C.'s Deposit Account

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Number 03-2769/2085-01700. If additional time extensions are needed, Applicants hereby petition for a second time extension and authorize the deposit account previously mentioned to be charged accordingly.

Respectfully submitted,



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